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Gallium Nitride Transistor Packaging Advances and Thermal Modeling

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Introduction

Gallium nitride-based transistor replacements for power MOSFETs have been widely available for over three years [1]. In addition to superior conductivity, these new-generation devices switch ten times faster than their aged silicon ancestors. The superior characteristics enable not only many new applications but also create more stringent requirements for packaging and thermal management. In this article, we discuss the advantages and thermal challenges of using the high performance enhancement mode eGaN® FETs in Land Grid Array (LGA) packages in high power density systems.

The Ideal Package

As low voltage silicon MOSFET performance has improved over the last number of years, the lack of high performance packaging has become a significant limiting factor, stimulating the development of such innovative packages as the DirectFET [2], and PolarPAK [3]. This leads to the question, what are the key requirements of a high performance package, and what is the “ideal” package?

Semiconductor devices are packaged in order to improve (a) robustness, (b) protection from the environment, and (c) ease of handling. At higher voltages, some packaging may also be needed to meet voltage clearance and creepage requirements. Packaging, however, degrades performance compared to the bare semiconductor die by adding to the manufacturing costs, increasing on-resistance, increasing inductance, increasing size, and degrading thermal performance.

What sets high performance packaging apart is their ability to realize the required advantages of device packaging while minimizing the drawbacks. At operating voltages below about 200 V, leadless, dual-side-cooled packaging such as DirectFET, PolarPAK, chip scale, or LGA becomes an elegant solution. Here the choice is largely dictated by the device's terminal structure; vertical vs. lateral. A lateral device lends itself to easy chip scale packaging (e. g. Great Wall's BGA MOSFETs [4]), while a vertical, "flipped" device needs to bring the high current substrate terminal down to the printed circuit board (such as DirectFET or PolarPAK). In a similar fashion, EPC's eGaN devices are in LGA packages (see Figure 1) where the interdigitation of source and drain terminals is used to minimize both on-resistance and parasitic inductance.

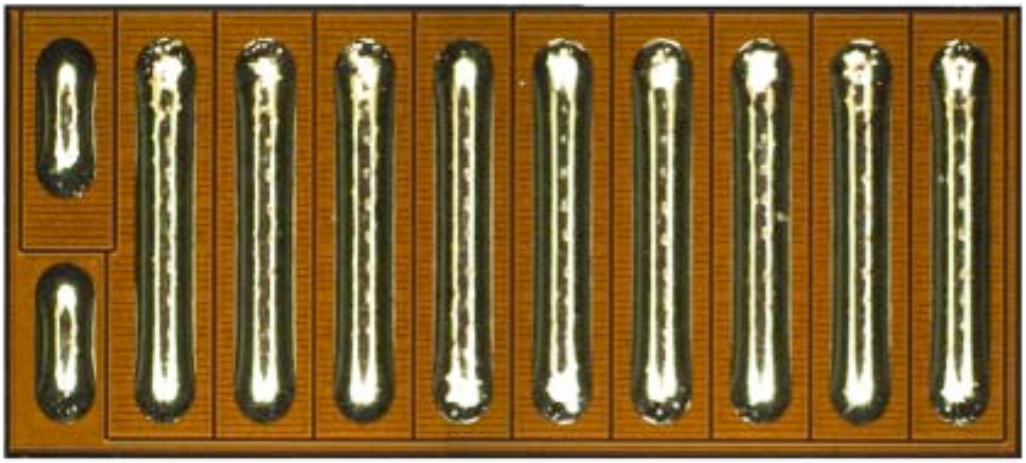

Figure 1: The EPC2001 eGaN FET is rated at 100 V, 7 mΩ and 25 A. This LGA package has a length of 4.1 mm and a width of 1.6 mm.

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Table 1 shows a comparison of the size of the eGaN FETs compared with equivalent on-resistance MOSFETs. The double advantage of the efficient chip scale LGA package and the smaller die size translate into a significant reduction on overall size occupied by the eGaN FET on a PCB.

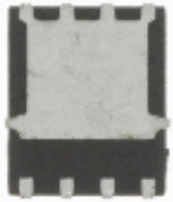
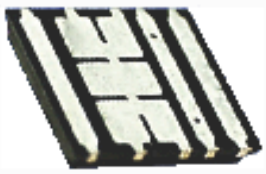
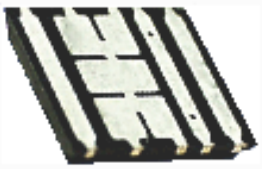
Device	LGA Package	Equivalent MOSFET Packages		
40 V 4 mΩ max	 4.1 x 1.6 mm	 5 x 6mm PQFN	 6.3 x 5 mm DirectFET®	 5 x 6 mm PolarPAK®
40 V 16 mΩ max	 1.7 x 1.1 mm		 4.8 x 3.9 mm DirectFET	
100 V 7 mΩ max	 4.1 x 1.6 mm			
100 V 30 mΩ max	 1.7 x 1.1 mm		 4.8 x 3.9 mm DirectFET	
200 V 100 mΩ max	 1.7 x 0.9 mm		 6.3 x 5 mm DirectFET	 5 x 6 mm PolarPAK

Table 1: Comparison between power MOSFETs in various packages and eGaN FETs in LGA packages.

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Package Resistance

The resistance of a power transistor package directly subtracts from the performance of the final product. The estimated packaging resistance of different standard power packages is shown in Figure 2 [5]. Added package resistance as low as a couple of hundred micro Ohms (not including PCB copper trace resistance) can be achieved in DirectFET, PolarPAK, and LGA package formats.

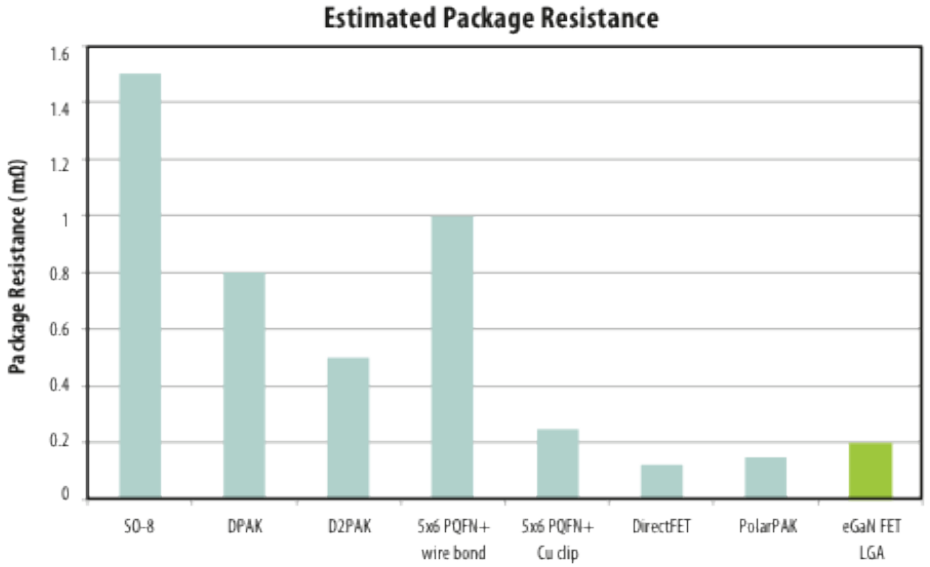

Figure 2: Estimated die free package resistance for different power packages (eGaN FET resistance is for EPC2001, EPC2015, and EPC2010. Smaller die have higher resistance).

Package Inductance

Package inductance can also degrade transistor and circuit performance; particularly when trying to switch in the nanosecond range [5]. The addition of package inductance can have varied effects, depending on which terminal of the die the package inductance is present. Common source inductance (inductance inside the package connected to the source terminal that carry both drain and gate return currents) can significantly increase switching losses by slowing down device switching through induced opposition of the applied gate voltage. A comparison of package inductance is shown in Figure 3 for the LGA compared to estimated values for some standard power packages.

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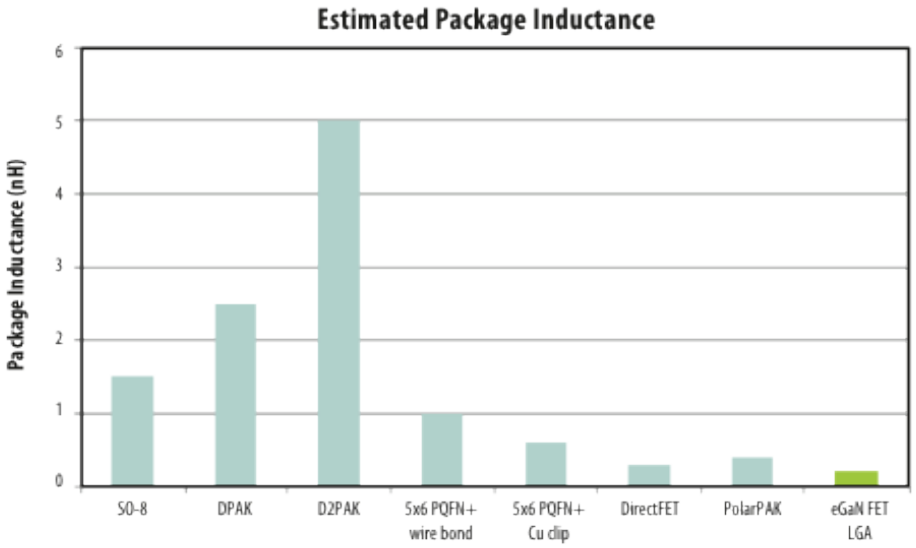

Figure 3: Estimated die free package inductance for different power packages. (eGaN FET inductance is for EPC2001, EPC2015, and EPC2010. Smaller die have higher inductance).

Package Thermal Resistance

Figure 4 illustrates the key components of thermal resistance in an LGA package. Heat is conducted away from the junction of the transistor either through the solder bars and into the circuit board, or upwards through the silicon substrate. If a heat sink is used, the heat must also pass through the thermal interface compound and through the heat sink. Referring to the thermal resistance values in Table 2 for the various eGaN FET part types, it can be seen that the thermal resistance to the back (silicon) surface of the mounted device is much lower than the thermal resistance to the PCB. Therefore, the designer can greatly enhance the power handling of the device by adding a heat sink as shown in Figure 4.

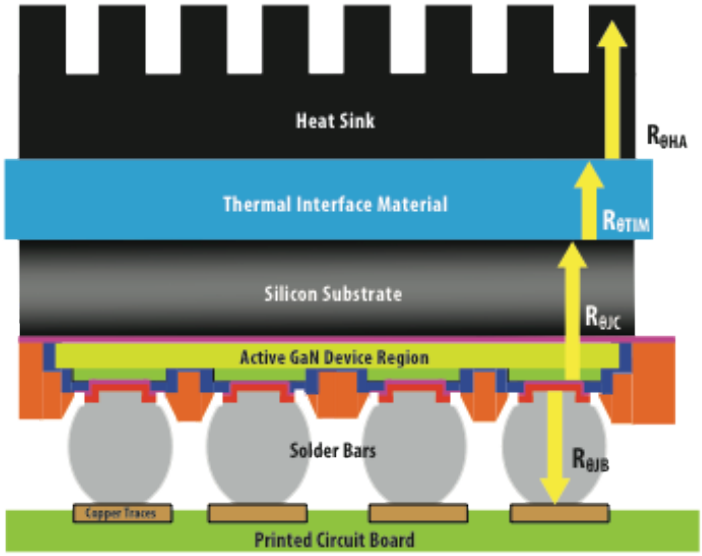

Figure 4: Not-to-scale cross-section of an eGaN FET mounted on a PCB and with a heat sink mounted on the top surface for additional cooling.

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Part Number	Side 1 (mm)	Side 2 (mm)	Die Area (mm²)	$R_{\theta JC}$ °C/Watt	$R_{\theta JB}$ °C/Watt
EPC2001	1.6	4.1	6.6	1.6	15
EPC2007	1.1	1.7	1.9	6.5	32
EPC2010	3.6	1.6	5.8	1.8	16
EPC2012	1.7	0.9	1.5	8.2	36
EPC2014	1.1	1.7	1.9	6.5	32
EPC2015	1.6	4.1	6.6	1.6	15

Table 2: eGaN FET Thermal Resistance [6]

To illustrate the difference in performance between a device with and without a heat sink, we first measured the junction temperature of the two EPC2007 eGaN FETs in an EPC9006 demo board configured as a buck converter with no heat sink. With 0.6 W of power being dissipated in each eGaN FET, the junction temperature reaches 70oC (see Figure 5) with an ambient temperature of around 28°C.

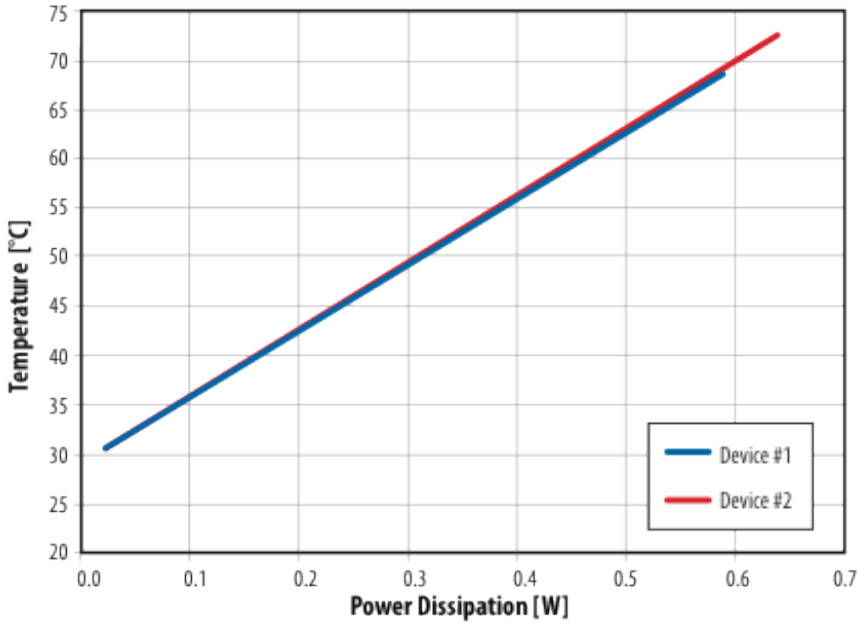

Figure 5: Without a heat sink and mounted on a standard FR4, 4-layer, 2 ounce copper PCB, the two EPC2007 eGaN FETs' junction temperatures rise to 70°C with 0.6 W of power dissipation in an ambient of 28°C.

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To improve the thermal performance, a 15 mm square and 9.5 mm tall finned heat sink was added above the eGaN FETs (see Figures 6 and 7). The heat sink datasheet gives a thermal impedance of 12 °C/W with an air flow of 200 LFM. In order to ensure adequate clearance between the heat sink and the 30-mil thick (762 microns) die, the heat sink was attached to the board using Gap Pad® GP 1500 (60 mils/1.5mm thick) [7] over half the heat sink area, while the area covering the eGaN FETs was filled using two layers of Sarcon 30x-m [8]. The two layers have a total thickness of 60 mils (1.5mm) and are able to conform around the die when compressed. This allows the die to conduct heat from the sidewalls as well as from the back surface. The heat sink was offset to barely cover the eGaN FETs such that the temperature of the PCB directly adjacent to the devices could be measured using a thermal infrared (IR) camera.

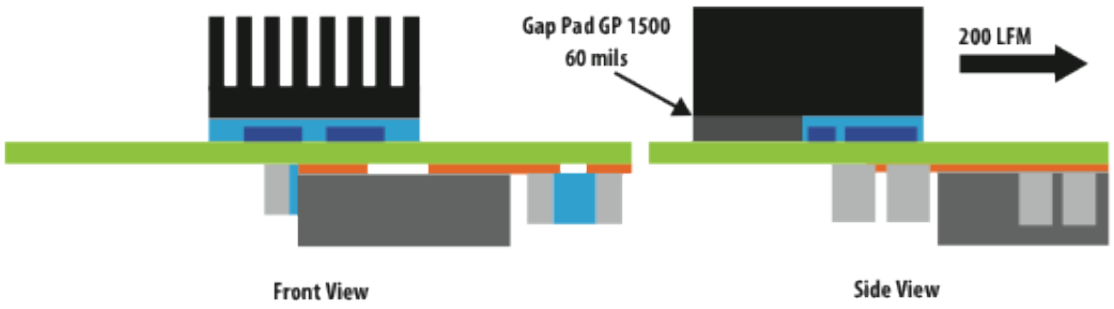

Figure 6: A 45 V to 22 V, 6 A, 4 MHz buck converter using EPC9006.

Figure 7: Standard (Left) and modified (Right) EPC9006 development boards.

Two analytic thermal models were developed using electrical-equivalent networks. The first of these models is shown in Figure 8 and is representative of the EPC9006 development board without a heat sink. Using the physical parameters illustrated in Figure 4, and the data sheet information for the EPC2007 from Table 2, a good fit to the measured data was obtained with the following additional assumptions:

1. The thermal resistance of the back surface of the eGaN FET to the ambient air with no airflow ($R_{\Theta CA1}$ and $R_{\Theta CA2}$ in Figure 8) is 133^{o}C/W;
2. The coupling thermal resistance between the two FETs mounted next to each other on the PCB (R2 and R3 in Figure 8) is 10^{o}C/W; and
3. The thermal resistance through the PCB to ambient (R5 in Figure 8) is 60^{o}C/W in still air.

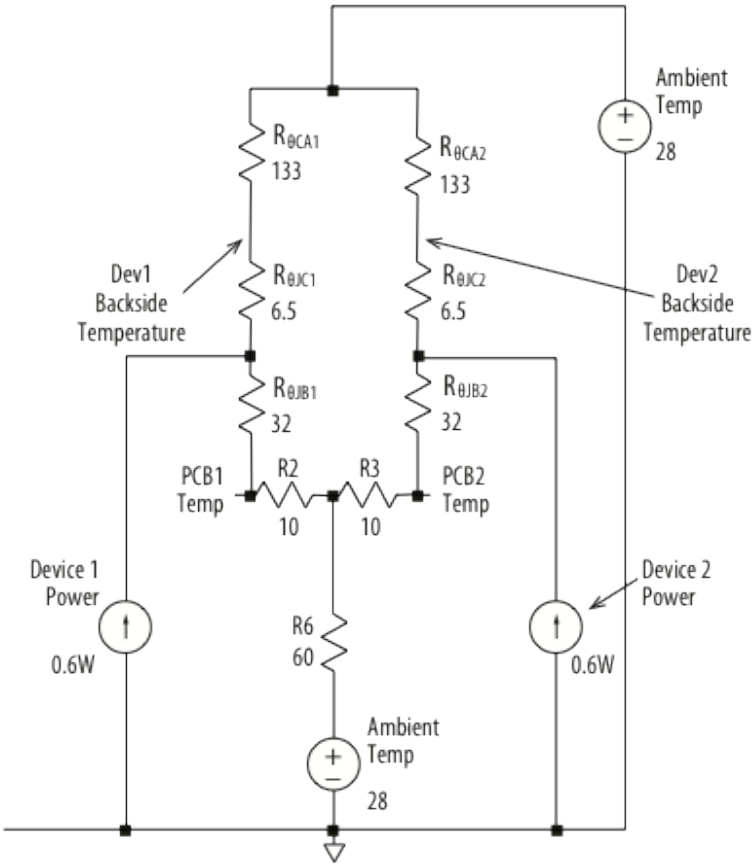

Figure 8: Electrical-equivalent circuit thermal model of the EPC9006 development board in still air without a heat sink.

The second model was based on the same EPC9006 development board, but configured as a high-frequency buck converter for use in an envelope tracking system [9]. In this case there are more elements on the PCB that dissipate power (due to the higher operating frequency); the most significant sources being the inductor [10] and the gate driver IC [11].

The heat sink has a thermal resistance ($R_{\Theta HA}$) of about 12°C/W (200 LFM airflow) and the thermal interface material has a thermal resistance ($R_{\Theta TIM}$) of about 5.5°C/W. Because the airflow is also blowing across the PCB, the effective PCB thermal resistance (R5) is reduced from 70°C/W (10 Ω in series with 60 Ω) down to 15°C/W (10 Ω in series with 5 Ω). In addition to the power dissipated in the two FETs, an additional input of power (I3) to the PCB of 1.82 W from the inductor and driver IC was included in the revised model.

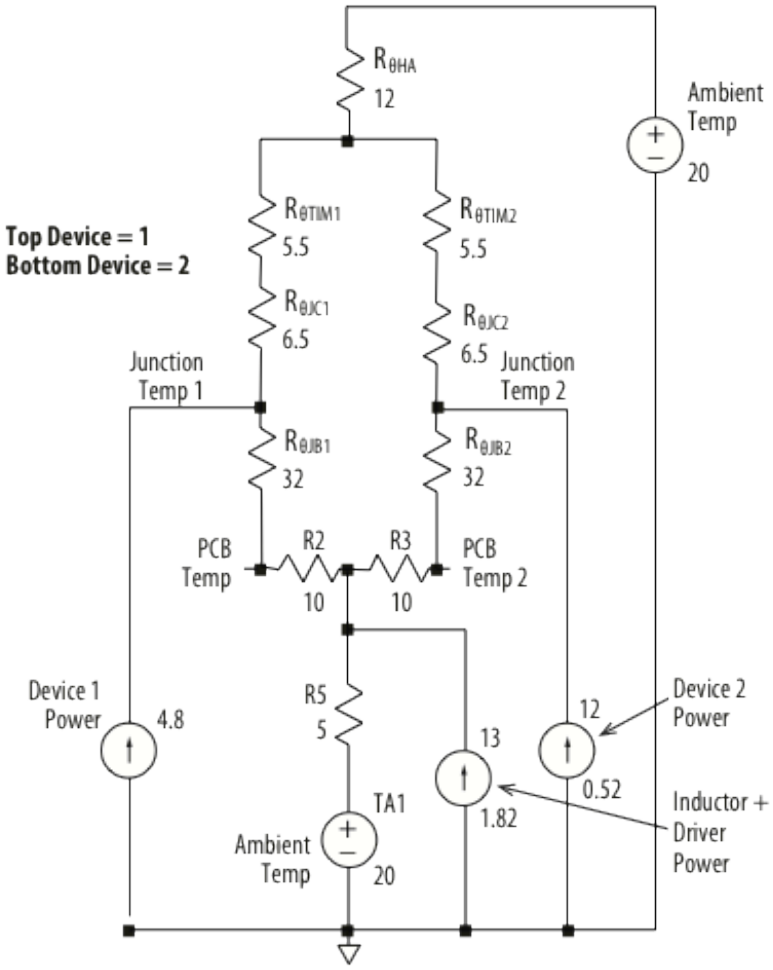

Figure 9: Electrical-equivalent circuit thermal model of the EPC9006 development board with a heat sink including power dissipation from the inductor and gate driver IC.

The model was tested by comparing the results to the actual operation of the circuit as a buck converter configured for 4 MHz with an input voltage of 45 V and an output voltage of 22 V (see Figure 10).

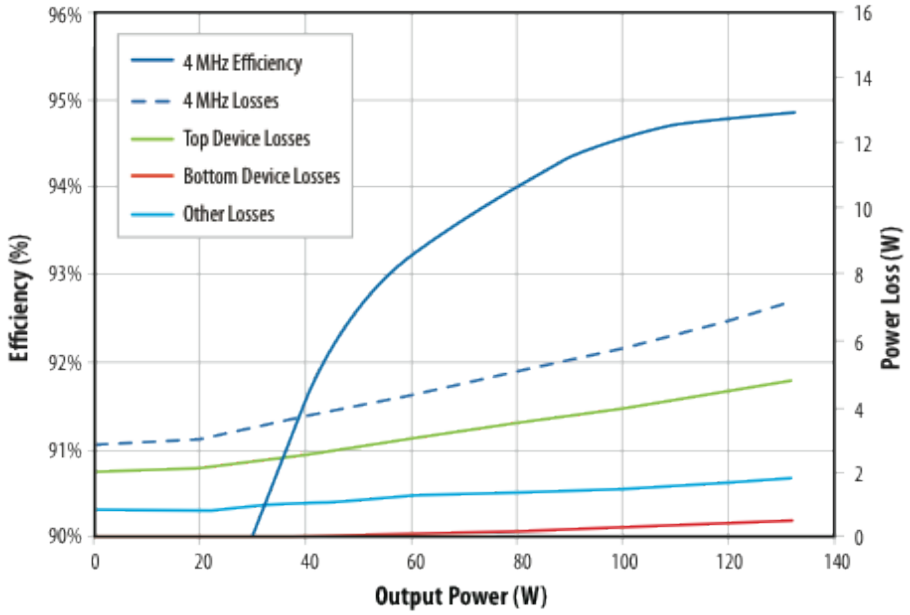

Figure 10: Efficiency and power loss of the EPC9006 demonstration board with a heat sink, operating at 4 MHz, 45 V_{IN}, 22 V_{OUT}.

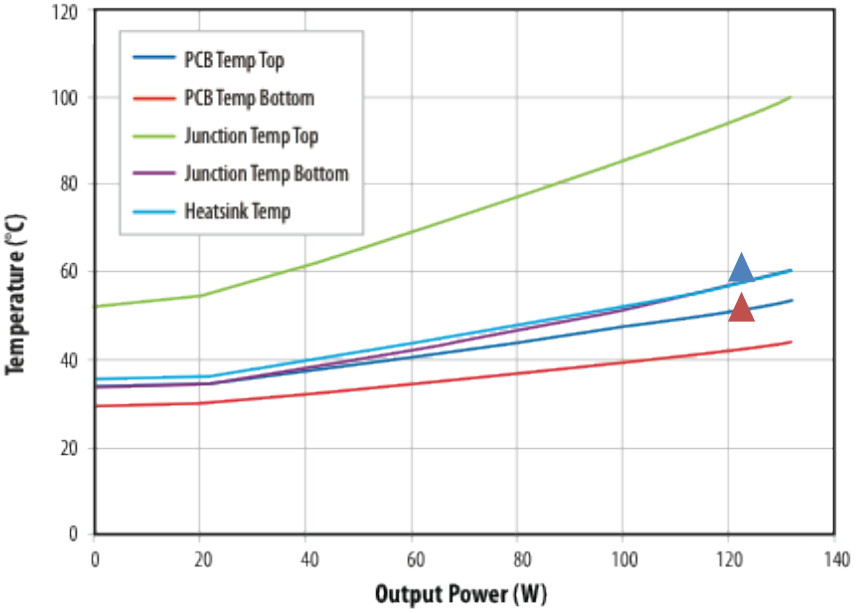

Figure 11: The temperatures of the PCB, heat sink, and device's junction with a heat sink and 200 LFM airflow. Triangles represent actual measured values.

Figure 11 plots the temperatures of the PCB, heat sink, and device's junction with a heat sink and 200 LFM airflow. The red triangle represents the PCB temperature, as measured by a thermal infrared (IR) camera, next to the bottom FET (Device #2) and the blue triangle represents the measured value for the PCB next to the top FET (Device #1). Figure 12 shows the estimated flow of dissipated power through the heat sink and through the PCB. Note that the upper FET is dissipating about ten times as much power as the lower FET (4.8 W vs. 0.5 W). This is due to the higher switching losses in the upper device. Of the 4.8 W, 3.3 W go out through the heat sink, and 1.5 W go out through the PCB – roughly in proportion to the relative thermal resistance of each path.

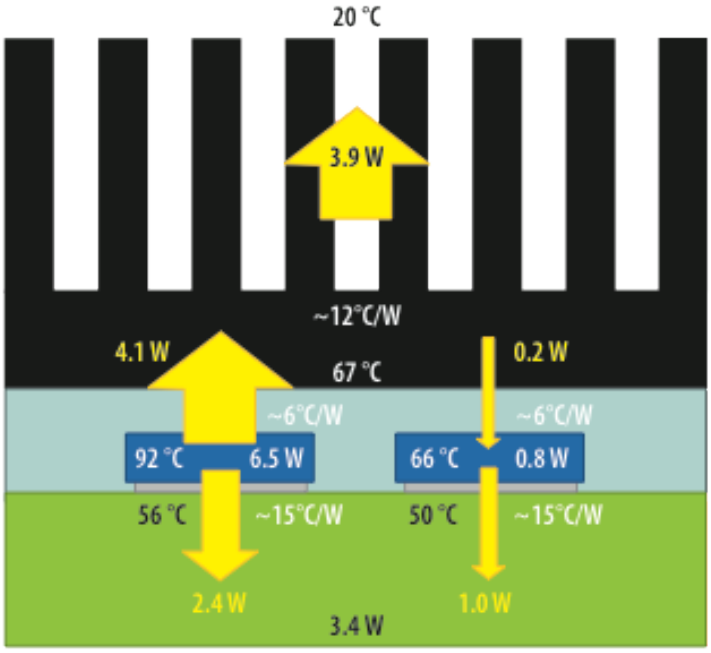

Figure 12: Estimated thermal diagram for the EPC9006 development board with a heat sink.

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Conclusions

eGaN FETs “packaged” in an LGA format fit many of the conditions as an ideal package. LGA packages have a minimum footprint on the PCB, and they have relatively no added resistance or inductance. This allows the designer to greatly shrink the size, and improve the efficiency of the power conversion system. With this reduced size, however, comes the problem of removing the heat generated from the increased power density. Simple heat sinking has been shown to greatly extend the capabilities of the eGaN FETs. From these experimental results we not only demonstrated a simple heat sink system that enhanced the power handling capability of the eGaN FETs by more than a factor of five, but also created an analytic model to predict the temperatures of the board, device’s junction, and heat sink resulting from actual circuit operation.

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